Specification Amendments

Please replace paragraph 0032 with the following rewritten paragraph:

0032 Overlying the first etching stop layer 16 is an insulating, inter-layer dielectric (ILD) layer 18 for subsequently forming a semiconductor feature, for example, a via and trench line, formed of, for example, low-k carbon doped silicon dioxide. The ILD layer 18 may be formed by a PECVD process although other processes well known in the art may be used. The ILD layer 18 (ILD layer) is deposited to a preferred thickness of between about 4000 and 10000 Angstroms. As device sizes shrink, typically a low-k (low dielectric constant material) with a dielectric constant of less than about 3 is used for the ILD layer 18 in order to reduce signal delay times due to parasitic capacitance effects. It will be appreciated, however, that conventional silicon dioxide may also be used as the ILD layer 18. Other exemplary materials that may be used to form the ILD layer include low-k organic materials applied by a spin coating process that are known in the art.

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